

In the Specification:

Please amend the paragraph bridging pages 7 and 8 as follows:

-- In addition, one or more of the “hit out” lines are connected to a “back-off” input on each processing agent 200. For one embodiment, a first processing agent 200 optionally includes a “back-off” input which is never asserted (e.g., the input is connected to logic zero). This processing agent 200 has the highest priority in an arbitration scheme described in detail below (i.e., no other agent ever tells this agent to “back-off”). A second processing agent 200 may include a “back-off” input which is connected only to the “hit out” of the first processing agent. This processing agent has the second highest priority (i.e., only the highest priority agent can tell this agent to “back-off”). If included in the system, a third processing agent 200 may include a “back-off” input which is connected to the output of a first OR gate 210. The inputs of the first OR gate 210 are in turn connected to the “hit out” signals of the first processing agent 200 and the second processing agent 200. This processing agent has the third highest priority (i.e., either of the highest priority agent and the second highest priority agent can tell this agent to “back-off”). If included in the system, a fourth processing agent 200 may include a “back-off” input which is connected to the output of a second OR gate 210. The inputs of the second OR gate 210 are in turn connected to the “hit out” signal of the third processing agent 200 and the output of the first OR gate 210. This processing agent 200 has the fourth highest priority (i.e., any of the first three agents can tell this agent to “back-off”). This pattern may continue for any number of processing agents 200 as shown in FIG. 2. From

the foregoing, persons of ordinary skill in the art will readily appreciate that, in the above example, the one or more OR gates 210 and the back-off inputs to the processing agents 200 are an arbitration circuit enforcing a fixed cache intervention priority between the caches 208. Thus, the one or more OR gates 210 and the back-off inputs are hardware which enforces a permanent hierarchy between the caches 208. This hierarchy is physically defined by the circuitry.--